drawings were further objected to for not showing the metal film recited in the claims. In response thereto, submitted for the Examiner's approval are proposed drawing corrections, in which Figures 10a and 10b have been labeled as prior art, and in which the wiring 706b has been indicated in Figure 9b. Moreover, the specification has been amended to reference the wirings 706a and 706b. Further, the claims that recited the metal film have been canceled, thus rendering this part of the objection moot. Upon allowance of the application and approval of the drawing changes, revised formal drawings will be submitted in compliance with United States Patent and Trademark Office guidelines. It is requested that these objections be withdrawn.

The Examiner has objected to the disclosure for various informalities. In response thereto, the disclosure has been amended to correct the informalities specifically noted by the Examiner, and to correct other informalities noted during the review. It is submitted that the specification complies with all official provisions, and it is requested that this objection be withdrawn.

The Examiner has rejected claims 1-4 as being obvious over the admitted prior art shown in Figures 10a and 10b in view of *Kajihara et al.* (USP 5,637,913). Because claims 2-4 have been canceled, Applicant will treat this rejection as pertaining only to independent claim 1, which has been amended to include the subject matter from canceled claim 3. It is submitted that this claim is patentably distinguishable over the cited references for at least the following reasons.

Applicant's independent claim 1 recites a semiconductor device which includes, *inter alia*, a semiconductor substrate, and reference lines that include an adhesive. The reference lines are disposed under a semiconductor element, and are respectively

provided at positions corresponding to at least three corners of the semiconductor element. The reference lines are adapted for use as a reference for determining a correct placement of the semiconductor element within an area of a circuit forming surface. This claimed configuration results in a semiconductor element that is more accurately placed, and it can be more easily adhered to a semiconductor substrate. This claimed device is neither disclosed nor suggested by the cited references.

Applicant's admitted prior art in Figures 10a and 10b do not disclose or otherwise suggest reference lines, much less reference lines that include an adhesive as recited in claim 1. Since the admitted prior art does not disclose or suggest such reference lines, then this admitted prior art likewise cannot possibly disclose or suggest reference lines that are adapted for use as a reference for determining a correct placement of a semiconductor element within an area of a circuit forming surface, as recited in claim 1.

The Examiner's Action relies on the teachings of *Kajihara et al.* to help overcome these deficiencies. However, *Kajihara et al.* do not disclose or suggest reference lines that include an adhesive, much less reference lines that are adapted for use as a reference for determining a correct placement of a semiconductor element within an area of a circuit forming surface of a semiconductor substrate. Instead, this patent only discloses forming projections 23 on leads for help in positioning a semiconductor chip on a die pad 3. There is no disclosure or suggestion of using these projections 23 as a reference for determining a correct placement of a semiconductor element within an area of a circuit forming surface of a semiconductor substrate, as recited within claim 1.

Further, although it is noted that the Examiner's Action has stated that the acknowledged prior art discloses on page 1, line 18 that reference lines are constituted

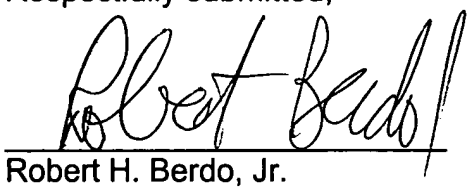
of an adhesive, it is noted that a careful reading of this passage will reveal that this is not the teaching from the admitted prior art. Instead, page 1, line 18 of Applicant's specification only discloses that the semiconductor element is secured with an adhesive, that is not shown, at the center of an upper surface of a substrate of the semiconductor device body. In fact, since the admitted prior art does not disclose or suggest reference lines (as acknowledged by the Action), then it is unclear how the Examiner's Action could possibly consider the prior art as teaching reference lines that are constituted of an adhesive. As such, it is submitted that the Examiner's Action has failed to establish a *prima facie* case of obviousness against at least original dependent claim 3, the subject matter of which is now corporated within independent claim 1. It is thus requested that this rejection be withdrawn, and that this claim be allowed.

Furthermore, Applicant has added an independent claim 19, which recites a method of mounting a semiconductor element on a substrate, and includes features similar to those recited within independent claim 1. These features are neither disclosed nor suggested by the cited references. It is likewise requested that this claim be allowed.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of the application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,



August 21, 2002
Date

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Please amend the specification as follows:

Page 3, line 22, through Page 4, line 18, please replace the section entitled "BRIEF DESCRIPTION OF THE DRAWINGS", with the following replacement section:

--The above and other features of the invention and the concomitant advantages will be better understood and appreciated by persons skilled in the field to which the invention pertains in view of the following description given in conjunction with the accompanying drawings which illustrate preferred embodiments. In the drawings:

[FIG.] FIGS. 1(a) and 1(b) presents top views of the structure adopted in the semiconductor device achieved in a first embodiment;

[FIG] FIGS. 2(a) and 2(b) presents top views of the structure adopted in the semiconductor device achieved in a second embodiment;

[FIG] FIGS. 3(a) and 3(b) presents top views of the structure adopted in the semiconductor device achieved in a third embodiment;

[FIG] FIGS. 4(a) and 4(b) presents top views of the structure adopted in the semiconductor device achieved in a fourth embodiment;

[FIG] FIGS. 5(a) and 5(b) presents top views of the structure adopted in the semiconductor device achieved in a fifth embodiment;

[FIG] FIGS. 6(a) and 6(b) presents top views of the structure adopted in the semiconductor device achieved in a sixth embodiment;

[FIG] FIGS. 7(a) and 7(b) illustrates the structure of the semiconductor device in the sixth embodiment;

[FIG] FIGS. 8(a) and 8(b) presents top views of the structure adopted in the semiconductor device achieved in a seventh embodiment;

[FIG] FIGS. 9(a) and 9(b) presents top views of the structure adopted in the semiconductor device achieved in an eighth embodiment; and

[FIG] FIGS. 10(a) and 10(b) presents top views of the structure adopted in the semiconductor device in the related art.--

Page 22, line 24, through Page 23, line 7, please replace the current paragraph with the following replacement paragraph:

--In addition, as shown in FIG. 9(b), a semiconductor element 702 is mounted at a specific position near the center of the surface of the substrate 701 constituting the semiconductor device main body by using the cross mark 703 and a frame portion 708 for reference and is secured with, for instance, an adhesive achieving a higher degree of accuracy. Electrode portions 704 at the mounted semiconductor element 702 are electrically connected to pad electrodes 705 on the substrate 701 constituting the semiconductor device main body via wirings 706a and 706b [706]. As in the semiconductor device in the related art, a specific area containing the semiconductor element 702 on the semiconductor substrate 701 is sealed with resin (not shown) and ball electrodes (not shown) which may be constituted of solder are formed at specific positions at the lower surface of the semiconductor device substrate 701.--

Page 24, line 12, through line 23, please replace the current paragraph with the following replacement paragraph:

--Next, the electrode portions 704 at the semiconductor element 702 accurately secured onto the semiconductor substrate 701 are electrically connected to the pad electrodes 705 on the substrate 701 at the semiconductor device main body through the wirings 706a and 706b which may be, for instance, gold wires. Subsequently, the specific area on the semiconductor substrate 701 containing the semiconductor element 702 and the pad electrodes at the periphery of the substrate is sealed with resin (not shown) as in the semiconductor device in the related art. In addition, the ball electrodes (not shown) which may be constituted of solder are formed at specific positions at the lower surface of the semiconductor substrate 701, thereby completing the process of manufacturing the semiconductor device in the embodiment.--

IN THE CLAIMS:

Please cancel claims 2-18 without prejudice or disclaimer to the subject matter recited therein.

Please amend the following claim:

1. (Amended) A semiconductor device, comprising[;]:

a semiconductor substrate [formed reference lines at] having a circuit forming surface, and having a plurality of electrode pads [with a pad electrode] provided on the circuit forming surface, said electrode pads being disposed to surround an area of the circuit forming surface; [at the periphery thereof, in correspondence to the positions of

at least three corners of a semiconductor element to serve as reference marks indicating positions at which semiconductor elements of varying sizes are to be mounted,]

a semiconductor element mounted within the area of the circuit forming surface; [at said circuit forming surface of said semiconductor substrate,]

reference lines that include an adhesive, said reference lines being disposed under the semiconductor element, and being respectively provided at positions corresponding to at least three corners of the semiconductor element, said reference lines being adapted for use as a reference for determining a correct placement of the semiconductor element within the area of the circuit forming surface; and

a sealing resin that seals [a specific area on said semiconductor substrate containing] said semiconductor element.